Robustness against Power is PSpace-complete

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Example (Message Passing Program)

Consider the multithreaded program (initially, $x = y = 0$):

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\begin{array}{c||c}
\text{Thread 1:} & \text{Thread 2:} \\
a\colon \texttt{mem}[x] \leftarrow 1 & c\colon \mathrm{r}_1 \leftarrow \texttt{mem}[y] \\
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Sequential Consistency (SC) [Lamport, 1979]

- Instructions are executed in order.
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$\Rightarrow$ The assumption holds.

Power Architecture by IBM et al. [Sarkar et al., 2011]

- Independent instructions can be executed out of order.
- Writes can be seen by different threads in different order.

$\Rightarrow$ The assumption does not hold.

Power Architecture 2/4

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$c : \mathsf{r}_1 \leftarrow \mathtt{mem}[y];\ d : \mathsf{r}_2 \leftarrow \mathtt{mem}[x].$

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Example (Thread 2 of Message Passing Program)

$c: \mathsf{r}_1 \leftarrow \mathtt{mem}[y];\ d: \mathsf{r}_2 \leftarrow \mathtt{mem}[x].$

Example (Computation of Thread 2)

$\beta := \mathsf{fetch}(c) \cdot \mathsf{fetch}(d) \cdot \mathsf{load}(c) \cdot \mathsf{load}(d) \cdot \mathsf{commit}(d) \cdot \mathsf{commit}(c).$

Power Architecture 3/4

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a: $\texttt{mem}[x] \leftarrow 1$; b: $\texttt{mem}[y] \leftarrow 1$.

Example (Computation of Thread 1)

$\alpha := \mathsf{fetch}(a) \cdot \mathsf{commit}(a) \cdot \mathsf{prop}(a, 1) \cdot \mathsf{fetch}(b) \cdot \mathsf{commit}(b) \cdot \mathsf{prop}(b, 1) \cdot \mathsf{prop}(b, 2)$.

Power Architecture 4/4

Example (Message Passing Program)

$$\text{Initially, } x = y = 0.$$

$$\begin{array}{c||c} \text{Thread 1:} & \text{Thread 2:} \\ a: \texttt{mem}[x] \leftarrow 1 & c: \mathsf{r}_1 \leftarrow \texttt{mem}[y] \\ b: \texttt{mem}[y] \leftarrow 1 & d: \mathsf{r}_2 \leftarrow \texttt{mem}[x] \end{array}$$

Assumption: $\mathsf{r}_1 = 1$ implies $\mathsf{r}_2 = 1$.

Example (Computation of the Program on Power)

$\tau := \alpha \cdot \beta = \mathsf{fetch}(a) \cdot \mathsf{commit}(a) \cdot \mathsf{prop}(a, 1) \cdot \mathsf{fetch}(b) \cdot \mathsf{commit}(b) \cdot \mathsf{prop}(b, 1) \cdot \mathsf{prop}(b, 2) \cdot \mathsf{fetch}(c) \cdot \mathsf{fetch}(d) \cdot \mathsf{load}(c) \cdot \mathsf{load}(d) \cdot \mathsf{commit}(d) \cdot \mathsf{commit}(c)$.

- Load c reads value 1 written by b.
- Load d reads the initial value 0, as store a was never propagated to Thread 2.

$\Rightarrow$ The assumption does not hold.

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Robustness Problem

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Reduce robustness checking to an emptiness check for an intersection of languages:

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- Language $\mathcal{L}$ consists of all normal-form computations.
- $\cap \mathcal{R}$ filters only violating computations.
- Decide $\mathcal{L} \cap \mathcal{R} \stackrel{?}{=} \emptyset$.

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Lemma ([Shasha and Snir, 1988])

A computation violates SC iff it has cyclic happens-before relation.

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Example (Happens-Before Relation of Computation τ)

	Thread 1	Thread 2
init_x	a: `mem`[x] $\leftarrow 1$	d: $\mathrm{r}_2 \leftarrow$ `mem`[x]
init_y	b: `mem`[y] $\leftarrow 1$	c: $\mathrm{r}_1 \leftarrow$ `mem`[y]

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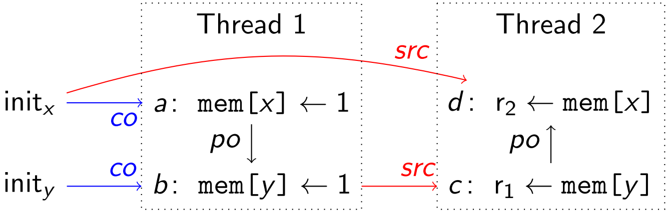

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- Source order — which store is read by which load.

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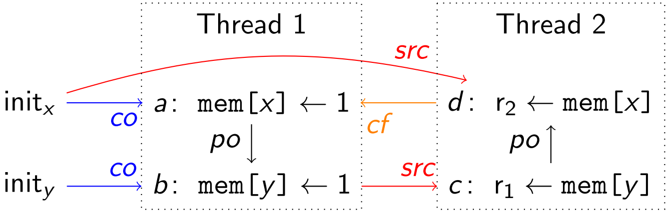

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- Program order — textual ordering of instructions.
- Coherence order — ordering of stores to the same address.
- Source order — which store is read by which load.
- Conflict order — which stores overwrite the value read by a load.

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Proof Idea.

Take a shortest computation with cyclic happens-before relation and transform it to the normal form. $\square$

Normal-Form Computations 2/4

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Given a non-empty valid computation, there is a thread, such that deletion of all events belonging to its last fetched instruction produces a valid computation.

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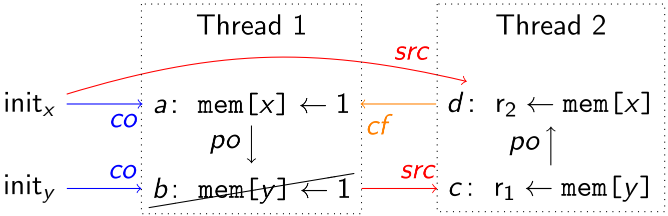

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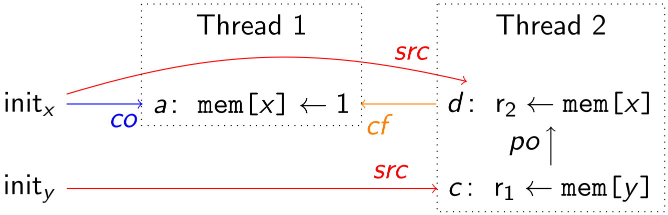

Normal-Form Computations 3/4

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Normal-Form Computations 4/4

Example

A shortest computation with cyclic happens-before relation:

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\begin{aligned}
\tau \quad = \quad & (\mathsf{fetch}(c) \cdot \mathsf{fetch}(d) \cdot \mathsf{fetch}(a)) \cdot \cancel{\mathsf{fetch}(b)} \\
\cdot \quad & (\mathsf{commit}(a) \cdot \mathsf{prop}(a, 1)) \cdot \cancel{\mathsf{commit}(b)} \cdot \cancel{\mathsf{prop}(b, 1)} \cdot \cancel{\mathsf{prop}(b, 2)} \\
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Matching sequentially consistent computation:

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Normal-form computation:

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Normal-Form Computations 4/4

Example

A shortest computation with cyclic happens-before relation:

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Generating Normal-Form Computations 1/2

Challenge

Describe the language $\mathcal{L}$ of all normal-form computations of a given degree.

Generating Normal-Form Computations 1/2

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Describe the language $\mathcal{L}$ of all normal-form computations of a given degree.

We need a language class that

- includes $\mathcal{L}$,
- is closed under intersection with regular languages ($\mathcal{L} \cap \mathcal{R}$),
- has decidable emptiness problem ($\mathcal{L} \cap \mathcal{R} \stackrel{?}{=} \emptyset$).

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Properties of $\mathcal{L}$

- Number of concurrently executed instructions is unbounded $\Rightarrow$ not regular.
- Can include computations like $(\text{fetch})^n \cdot (\text{load})^n \cdot (\text{commit})^n$ $\Rightarrow$ not even context-free.

Generating Normal-Form computations 2/2

Solution

Define $\mathcal{L}$ as a language of a multiheaded automaton.

Generating Normal-Form computations 2/2

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Definition (Multiheaded Automaton)

An *n*-headed automaton is an extension of NFA generating n parts of a computation simultaneously, one by each head.

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Example (Generating τ'' with a 3-headed Automaton)

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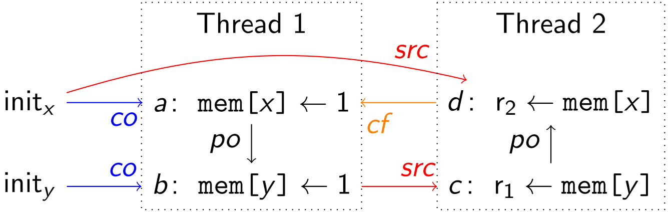
Checking Cyclicity of Happens-Before Relation

Example (Happens-Before Relation of τ'')



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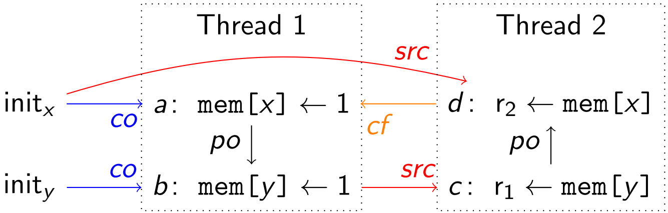

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- The multiheaded automaton in each thread picks two instructions in program order.

Checking Cyclicity of Happens-Before Relation

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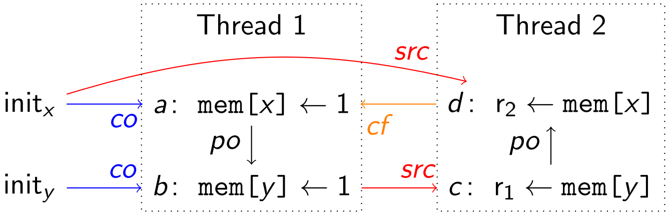

Solution

- The multiheaded automaton in each thread picks two instructions in program order.
- Finite automata check edges between picked instructions from different threads.

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Theorem

Assuming finite memory, robustness is PSPACE-*complete.*

Proof.

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- Upper bound: $\mathcal{L} \cap \mathcal{R} \stackrel{?}{=} \emptyset$.

Complexity

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- Upper bound: $\mathcal{L} \cap \mathcal{R} \stackrel{?}{=} \emptyset$.
- Lower bound: SC state reachability [Kozen, 1977].

$\square$

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- Robustness
  - Characterization: [Shasha and Snir, 1988].
  - Monitoring algorithms:
    - [Burckhardt and Musuvathi, 2008] (TSO-only, broken),
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  - Static overapproximation and fence insertion:
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- Power models:
  - [Sarkar et al., 2011] (operational),
  - [Mador-Haim et al., 2012] (axiomatic),
  - [Alglave et al., 2013] (overview, newer axiomatic),
  - [Maranget et al.,] (tutorial, with ARM).

Summary

Reduction of Robustness to Language Emptiness

- Look only for normal-form violating computations.
- Use multiheaded automata to generate normal-form computations.
- Check cyclicity of happens-before by regular intersection.

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Robustness against Power is PSPACE-complete

- Upper bound: reduction to language emptiness.
- Lower bound: sequentially consistent state reachability.

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Thank you for your attention.
Questions?
derevenetc@cs.uni-kl.de

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